UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/596,401	06/12/2006	**Valeri Dimitrov Ivanov**	60291.000046	6178

21967 7590 05/28/2009

HUNTON & WILLIAMS LLP
INTELLECTUAL PROPERTY DEPARTMENT
1900 K STREET, N.W.
SUITE 1200
WASHINGTON, DC 20006-1109

EXAMINER	
BUI, THA-O H	

ART UNIT	PAPER NUMBER
2824	

MAIL DATE	DELIVERY MODE
05/28/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/596,401	IVANOV ET AL.	
	Examiner	Art Unit	
	THA-O BUI	2824	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 June 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9* is/are pending in the application.

4a) Of the above claim(s) *6* is/are withdrawn from consideration.

5)☒ Claim(s) *3;9* is/are allowed.

6)☒ Claim(s) *1,2,4,5,7 and 8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 June 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *02/25/2008*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Preliminary Amendment

1. Acknowledgment is made of applicant's Preliminary Amendment, filed 04 November 2008. The changes and remarks disclosed therein were considered.

Claim 6 has been cancelled and claim 9 has been added by Amendment. Therefore, claims 1-5, 7-9 are pending in the application.

Information Disclosure Statement

2. Acknowledgment is made of applicant's Information Disclosure Statement (IDS) Form PTO-1449, filed 25 February 2008. The information disclosed therein has been considered.

Specification

3. The disclosure is objected to because of the following informalities:

In page 9, lines 4, "Used is a 0.6 m BiCMOS EPROM" should be understood --Used is a 0.6 μm BiCMOS EPROM--.

5. Claims 5 and 8 are objected to because of the following informalities:

Said claim 5 depends on claim 4 which appears to be in error due to "said supply in said static mode but said program voltage" lacking antecedent basis. It will be understood to depend on claim 3, and it will be understood --a supply in said static mode but said program voltage--.

In claim 8 which appear to be in error due to "the supply voltage in static mode". It will be understood --a supply voltage in static mode--.

Appropriate correction is required.

6. Claim 7 is objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form. ---the method comprising---.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 1-2, 4-5, 7-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Randazzo (U.S Patent No. 5648930) in view of Countryman, Jr (U.S Patent No. 4573144 hereinafter "Countryman").

Regarding claim 1, Randazzo, for example in Fig. 5, discloses that a bi-stable latch circuit having a pair of cross-coupled branches (72; 74, in Fig. 5), each branch including a complementary driver (including 82;148) and a load (80) connected between a drain line (76) and a source line (78), and each branch also including a non-volatile memory cell having a program transistor and a read transistor (82; 86), comprising; at least one of the drivers and loads includes a corresponding read transistor (branch [72], in Fig. 5); said driver and load of said branch are connected in series at a respective output node (branch [72], node [93, 94] are

input/output node; in Fig. 5); said read transistor and program transistor have a common floating gate (having a floating gate [82]) and separate control gates; said control gate of said program transistor is connected to a program voltage (i.e., input/output node [93; 94] in Fig. 5); the drain of said program transistor connected to a respective input node (i.e., the input/output node [93; 94] in Fig. 5); and said control gate of said read transistor in said branch is connected to the output node of the other branch (i.e., read transistor [82; 86] in said branch [72; 74] in Fig. 5).

Randazzo does not disclose a common floating gate which performs control for programming the nonvolatile latch.

However, Randazzo discloses such a method of programming a binary state in a nonvolatile memory (see Fig. 5 and Col. 2, lines 57-67; Col. 4, lines 57-67; Col. 5, lines 1-15).

Also, Countryman, for example in Fig. 8, discloses a common floating gate (as implied in Col. 1, lines 17-48, and lines 59-68) which performs control for programming a floating gate transistor which share a common floating gate transistor (see in Figs. 3-4, and 8 of Countryman) is used to selectively provide hot electron injection (see abstract, Col. 2, lines 45-68).

Since the operation of Countryman's EEPROM is similar to that of Randazzo's the nonvolatile element latches the memory circuit (see for example in Col. 2, lines 3-27), and programming a common floating gate was common and well known in the art (as in Countryman), and Randazzo discloses that a memory cell for programming, it would have been obvious at the time the invention was made to a person having ordinary skill in the art to modify the Randazzo's the nonvolatile element latches the memory circuit such that a common floating gate programming circuit (as in Countryman), for the purpose of avoid having high voltage adversely effect the decoder circuit (see for example in Col. 17-48).

Regarding claim 2, the above Randazzo/Countryman combination further discloses that wherein at least one of said read transistor or program transistor is a semiconductor device using hot electron injection for changing a threshold voltage thereof (see for example of Countryman in Fig. 8, Col. 2, lines 45-68).

Regarding claim 4, the above Randazzo/Countryman combination further discloses that wherein the inputs are held at logic low level (i.e., the pair of invertors [72; 74] or latch in Fig.5 of Randazzo) in said static mode but the voltage at one of said inputs is raised to a voltage high enough to generate hot electrons or hot holes at the drain of a respective program transistor in a program mode (i.e., To program, a high voltage is applied at [V.sub.PP] while high voltage select signal [SP] is applied to transistor [72]. Current thus flowing through transistor [71] produces hot electrons which are collected by floating gate [73] which in turn causes transistor [69] to increase in threshold voltage; in Fig. 8 of Countryman; Col. 5, lines 50-68; Col. 6, lines 1-20).

Regarding claim 5, the above Randazzo/Countryman combination further discloses that wherein said program voltage (i.e. program voltage [Vpp] in Fig. 8 of Countryman) is connected to said supply voltage in said static mode but said program voltage is raised to a voltage high enough to attract electrons or holes into said floating gate in said program mode (see for example in Fig. 8 of Countryman; Col. 5, lines 50-68; Col. 6, lines 1-20).

Regarding claim 7, Randazzo, for example in Fig. 5 discloses that a method for programming (see for example in Abstract) a bi-stable latch circuit (146, in Fig. 5), the bi- stable latch circuit having a pair of cross-coupled branches (72; 74), each branch including a complementary driver (including 82; 148) and a load (80) connected between a drain line (76) and a source line (78), and each branch also including a non-volatile memory cell (82, 86) having a program transistor and a read transistor (82, 86), comprising according to claim 1 comprising; holding the input (i.e., the input/output node [93, 95] in Fig. 5), voltages at logic low level in a static mode (78); and raising the input voltages to a voltage high enough to generate hot electrons or hot holes at the drain of a respective transistor in a program mode.

Randazzo does not disclose the input voltages to a voltage high enough to generate hot electrons at the drain of a respective transistor in a program mode.

However, Randazzo disclose such the floating gate transistor [82] and [86] are programmed when a sufficient number of electrons are injected from the drain-source channels (see for example in Col. 5, lines 16-35).

Also, Countryman, for example in Fig. 8, discloses a programmable link transistor (see for example in Fig. 8, Col. 5, lines 50-68; Col. 6, lines 1-20).

Since the operation of Countryman's EEPROM is similar to that of Randazzo's the nonvolatile element latches the memory circuit (see for example in Col. 2, lines 3-27), and the input voltages to a voltage high enough to generate hot electrons at the drain was common and well known in the art (as in Countryman), and Randazzo discloses that a method of programming, it would have been obvious at the time the invention was made to a person having ordinary skill in the art to modify the Randazzo's the nonvolatile element latches the memory circuit such that a programmable link transistor (as in Countryman), for the purpose of avoid having high voltage adversely effect the decoder circuit (see for example in Col. 17-48)

Regarding claim 8, the above Randazzo/Countryman combination further discloses that comprising: connecting the program voltage to supply voltage in mode (i.e., applying a program voltage Vpp voltage; in Fig. 8 of Countryman); and raising program voltage to a voltage high enough to attract electrons or holes into the floating gate in program mode (see for example in Fig. 8 of Countryman; Col. 5, lines 50-68; Col. 6, lines 1-20).

Allowable Subject Matter

4. Claims 3 and 9 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

5. The following is a statement of reasons for the indication of allowable subject matter:

Regarding claims 3 and 9, the prior art of record fail to teach or suggest a bi-stable latch circuit as recited in claims 3 and 9, and particularly, in conjunction with other limitation, a common supply voltage in static mode but at least one of said drain and source line is disconnected from said common supply voltage in a program mode.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to THA-O BUI whose telephone number is (571)270-7357. The examiner can normally be reached on Monday Through Friday, 8:00 to 5:00 Alternate Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on 571-272-1869. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/TB/
05/20/2009

/J. H. Hur/ 5/26/2009
Primary Patent Examiner, Art Unit 2824